INDIAN INSTITUTE OF TECHNOLOGY PALAKKAD
Proforma for Proposing Course (New)

Course Code/ Title	**CS5xxx Advanced Computer Architecture**[1]		
Program	M.Tech SoCD		
Course Credits	3-0-0-3		
Course Category	PMT		
Prerequisite	A basic course on Computer Organization/Architecture		
Consent of Teacher	Not Required		
Date of Proposal	14-02-2020	Date of Approval	
Proposing Faculty	Dr. Sandeep Chandran and Dr. Vivek Chaturvedi		

Course Contents

S. No	Topic	Hours
1	**Design Space Exploration and Optimizations:** Performance metrics and performance enhancement techniques, Basic concepts of parallel processing and pipelining, Power dissipation in processors, power metrics, and low-power design techniques.	6
2	**Instruction set architecture design:** Instruction set design, implementation and performance perspectives, relative advantages of RISC and CISC instruction set, Data Path Design,	6
3	**Instruction-level parallelism (ILP):** Pipeline data-path, data-dependence. Challenges in ILP realization. Pipeline hazards and their solutions, out-of-order execution, branch prediction, and dynamic scheduling. VLIW and superscalar processors.	12
4	**Memory systems:** Overview of memory hierarchy, Cache design considerations, instruction vs. data caches, write-policy and replacement policy, analysis of cache performance, and cache design for performance enhancement. Brief overview of memory technologies (SRAM, DRAM, and flash).	12

[1] This course will replace another course offered under the same name by the CSE Department (CS4505: Advanced Computer Architecture). The original course will be discontinued going forward. The syllabus of this course is tailored to suit graduate students.

5	**Data Level Parallelism:** Flynn Processor classification, SIMD, MIMD, GPU architectures	4
6	**IO:** types, models, protocols, Sockets, ISR	2
	Total Hours	42

Learning Objective

- Teach advanced design principles of modern processors by addressing key issues such as instruction set design, micro-architecture of superscalar processors, its interaction with other hardware components, and constraints to be addressed when going from single-core to multi-core systems
- Teach students different techniques to estimate, analyze and enhance performance as well as reduce power dissipation of computing systems.

Learning Outcome

Upon successful completion of the course, students would be able to:

- Interpret the performance of a processor based on metrics such as execution time, cycles per instruction (CPI), Instruction count etc
- Predict the challenges of realizing different kinds of parallelism (such as instruction, data, thread, core level) and leverage them for performance advancement
- Apply the concept of memory hierarchy for efficient memory design and virtual memory to overcome the memory wall
- Explore emerging computing trends, computing platforms, and design trade-offs

Teaching Methodology: Depends on the Instructor(s)

Assessment Methods: Depends on the Instructor(s)

Text Books

1. J.L.Hennessy, D.A.Patterson, Computer Architecture: a quantitative approach, Morgan Kaufmann, 5th edition, 2011, ISBN: 978-1558605961.
2. William Stallings, Computer Organization and Architecture, Prentice Hall, 10th edition, 2015, ISBN-10: 013293633X, ISBN-13: 978-0132936330

Reference Books

1. Andrew S. Tanenbaum, Structured Computer Organization, Prentice Hall, 6th edition, 2012, ISBN: 978-0132916523.
2. Patterson, J.L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, Morgan Kaufmann, 5th edition, 2013, ISBN-13:9780124078864
3. C. Hamacher, Z. Vranesic and S. Zaky, Computer Organization, McGraw-Hill, 5th edition,2002, ISBN: 0072320869.

INDIAN INSTITUTE OF TECHNOLOGY PALAKKAD
Proforma for Proposing Course (New)

Course Code/ Title	**CS5xxx Advanced Computer Architecture Lab**		
Program	M.Tech SoCD		
Course Credits	0-0-3-2		
Course Category	PML		
Prerequisite	A basic course on Computer Organization/Architecture		
Consent of Teacher	Not Required		
Date of Proposal	04-03-2020	Date of Approval	
Proposing Faculty	Dr. Sandeep Chandran and Dr. Vivek Chaturvedi		

Course Contents

This is the companion lab of Advanced Computer Architecture (PMT of M.Tech SoCD).
The experiments would be done using a state-of-the-art, open-source architectural simulator.

Learning Objective

- Same as Advanced Computer Architecture

Learning Outcome

- Same as Advanced Computer Architecture

Teaching Methodology: Depends on the Instructor(s)

Assessment Methods: Depends on the Instructor(s)

Text Books

1. J.L.Hennessy, D.A.Patterson, Computer Architecture: a quantitative approach, Morgan Kaufmann, 5th edition, 2011, ISBN: 978-1558605961.
2. William Stallings, Computer Organization and Architecture, Prentice Hall, 10th edition, 2015, ISBN-10: 013293633X, ISBN-13: 978-0132936330

Reference Books

1. Andrew S. Tanenbaum, Structured Computer Organization, Prentice Hall, 6th edition, 2012, ISBN: 978-0132916523.

2. Patterson, J.L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, Morgan Kaufmann, 5th edition, 2013, ISBN-13:9780124078864
3. C. Hamacher, Z. Vranesic and S. Zaky, Computer Organization, McGraw-Hill, 5th edition,2002, ISBN: 0072320869.

INDIAN INSTITUTE OF TECHNOLOGY PALAKKAD
Proforma for Proposing Course (New)

Course Code/ Title	**CSxxxx Programming Lab**		
Program	M.Tech SoCD		
Course Credits	1-0-3-3		
Course Category	PML		
Prerequisite	none		
Consent of Teacher	Not required		
Date of Proposal		Date of Approval	
Proposing Faculty	Dr. Unnikrishnan		

Course Contents

S. No	**Topic**	**Hours**
1	Linux basics, version control, coding styles,	4
2	Coding conventions, debugger, and build system such as Makefiles	8
3	Scripting: Python, Shell (Bash,Csh), Tcl	12
4	Processes,Linker, Loader, Memory Layout, Static and Dynamic Linking	12
5	Multi-Processing: Shared and distributed systems overview. Parallel Programming with Pthreads, OpenMP and MPI	16
	Total Hours	52

Learning Objective

- Equip students with system tools that improve productivity.
- Exposure to advanced programming constructs.
- Equip students to work on cluster/remote-machines using command line (bash/csh).
- Exposure on proper usage of hardware resources like CPU cores, memory in programs.

Learning Outcome

- Familiarity to work on open source systems from source code compilation.
- Familiarity to work on group projects with proper version control.
- Parallel programming skills for multi-core CPU clusters.
- Familiarity on how processes are mapped to machines.

Teaching Methodology: Depends on the Instructor(s)

Assessment Methods : Depends on the Instructor(s)

Text Books

1. Linux Command Line and Shell Scripting Bible. Author: Richard Blum. Publisher: Wiley Publishing. ISBN-10: 111898384X, ISBN-13: 978-1118983843

2. Parallel Programming in C with MPI and Openmp, Author: Michael Quinn. Publisher: McGraw-Hill Education. ISBN-10: 0071232656, ISBN-13: 978-0071232654.

Reference Books

1. The Unix Programming Environment, Authors: Brian W Kernighan and Rob Pike. Publisher: Pearson. ISBN-10: 9332550255, ISBN-13: 978-9332550254.

2. An Introduction to Parallel Programming. Author: Peter Pacheco. Publisher: Morgan Kaufmann Publishers. ISBN-13: 978-0-12-374260-5

INDIAN INSTITUTE OF TECHNOLOGY PALAKKAD

Proforma for proposing MTech course (New)

Course Code and Title	**EE5XXX: VLSI Design**				
Programme	**B.Tech/MS/M.Tech/PhD**	**Year of study**		**Semester**	
Course credit	**3-0-2-4**				
Course category	**PMT (MTech) and PME (for BTech/MS and PhD)**				
Prerequisite, if any	Digital Systems				
Consent of teacher, if required	**No**				
Date of proposal	**9 Nov. 2019**	**Date of Senate Approval**			
Proposing faculty	**Subrahmanyam Mula**				

Course Description:

This course will introduce the design and implementation issues of IC Design. The course emphasizes on the key factors for modern chip design: delay, power, interconnect, and robustness. This course focuses on building an understanding of integrated circuits from the bottom up from a fundamental understanding of circuit and physical design. Detailed course content is given below:

Course Content

S/N	Topic	Lecture (hours)	Lab (hours)
1	***Fundamentals*** Motivation and scope of the course; General overview of design hierarchy, layers of abstraction, VLSI design styles, packaging styles, design automation principles, Process variation and robustness; VLSI Scaling issues	4	0
2	***CMOS inverter Characteristics*** DC transfer characteristics, noise margins, linear delay model and logical effort, timing analysis delay models; Interconnect modelling, logical effort with wires; CMOS inverter layout and circuit simulation	9	6
3	***CMOS Power Consumption*** Dynamic power, static power, energy-delay optimization, pipelining, parallel processing low power design techniques, overview of circuit families;	9	8

4	***System design issues*** Design of arithmetic building blocks adders and multipliers, barrel and logarithmic shifters; sequential design issues, max-delay/min-delay constraints, time borrowing, clock skew, characterizing sequencing element methodology, multiple clock domains and synchronizers, FIFO design, Verilog design examples.	10	10
5	***Memory and I/O design*** Dynamic Random-Access Memories (DRAM), Static RAM, non-volatile memories, flash memories, low-power memory; Robust memory design, power distribution, clock distribution, I/O and high-speed links.	10	4
	TOTAL	42	28

Learning Outcomes:

At the end of the course, the students should be able to

- Understand the VLSI design flow starting from architecture design, microarchitecture design, logic design, circuit design, and finally physical design
- Understand the area-power-speed tradeoffs involved in designing a modern IC.
- Be familiar with effect of this feature size scaling on chip performance and design methodologies.

Teaching Methodology: Classroom lectures and Lab exercises

Assessment Methods: Written examination and continuous lab assessment

Text Books

1. Neil Weste and David Harris, CMOS VLSI Design: A Circuits and Systems perspective", Pearson Education India, 4th edition, 2010, **ISBN-13:** 978-0321547743,
2. J. M. Rabaey, A. Chandrakasan, and B. Nikolic, —Digital Integrated circuits: A design perspective‖ 2nd Edition, Pearson Education India, 2016. **ISBN-13:** 978-9332573925

INDIAN INSTITUTE OF TECHNOLOGY PALAKKAD

Proforma for course

Course Code and Title	EE5XXX Nanoelectronics for Circuits and Systems				
Programme	M.Tech/MS/PhD	**Year of study**		**Semester**	
Course credit	3-0-0-3				
Primary Course category	PMT (M.Tech, SoCD)				
Prerequisite course, if any	Nil				
Consent of teacher, if required	Not required				
Date of proposal	February 11, 2020	**Date of Senate Approval**			
Proposing faculty	Revathy Padmanabhan				

Course Content

Sl. No.	Topic	Lecture (hours)
1	***Introduction and Fundamentals*** Equilibrium carrier concentration; intrinsic and extrinsic semiconductors: Band model; Recombination-generation; Semiconductor equations: carrier transport, continuity and Poisson equations, boundary conditions.	12
2	***MOS junctions and transistors*** Metal-oxide-semiconductor (MOS) junction: C-V characteristics, threshold voltage, body effect; MOS field-effect transistors (MOSFETs): characteristics and modelling; basic planar Complementary MOS (CMOS) process flow.	7
3	***CMOS scaling*** Overview of International Roadmap for Devices and Systems (IRDS); Moore's law, short channel effects and solutions to overcome it; modern day MOSFETs.	8
4	***Memory technologies*** Overview of 3D crossbar array; scaling of memories; volatile Dynamic Random Access Memory (DRAM): design of single DRAM cell; non-volatile memories: flash memory; Emerging memory technologies.	7
5	***Compact modeling*** Introduction to compact modeling for circuit simulation; overview of BSIM MOSFET model; sample transistor process design kit (PDK).	8
	TOTAL	42

Learning Objectives:

This is an introductory course in the area of device design and modeling, as applied to modern transistor-based circuits and systems, with a focus on devices for computing and memory applications. The objective of this course is to give the students a flavour of the challenges in the design of ultra-scaled transistors; so that they will be able to appreciate the need for understanding device behaviour, in order to analyse the performance of circuits and systems. Students will also be introduced to transistor process design kits, and their use in electronic system design.

Learning Outcomes:

At the end of the course, students should be able to:

- understand the behaviour of MOS-based devices, and have an overview of the processes involved in the fabrication of integrated circuits.
- analyse the impact of device scaling on the performance of computing and memory systems.
- appreciate the role of device modeling in order to facilitate circuit and system design.

Teaching Methodology : Classroom lectures

Assessment Methods : Written examinations/quiz, continuous assessment

Text Books:

1. T. A. Fjeldly, T. Ytterdal, and M. S. Shur, "Introduction to Device Modeling and Circuit Simulation," Wiley-Interscience, ISBN-13: 978-0471157786.
2. Y. Taur and T. H. Ning, "Fundamentals of Modern VLSI Devices," Cambridge University Press, ISBN-13: 9780511601538.
3. B. G. Streetman and S. Banerjee, "Solid State Electronic Devices," Pearson Education India; Seventh edition (2015), ISBN-10: 9332555087, ISBN-13: 978-9332555082.

References:

1. International Roadmap for Devices and Systems: https://irds.ieee.org/.
2. Y. Tsividis, "Operation and Modeling of the MOS Transistor," The Oxford Series in Electrical and Computer Engineering, ISBN-13: 978-0195170153, ISBN-10: 0195170156.
3. R. F. Pierret, "Semiconductor Device Fundamentals," Pearson 2nd edition, ISBN-10: 0201543931, ISBN-13: 978-0201543933.
4. N. Bhat, S. A. Shivashankar, and K. N. Bhat, "Nanoelectronics: Devices and Materials," NPTEL video lectures: [link].
5. S. Karmalkar, "Solid state devices," NPTEL video lectures: [link]
6. M. A. Alam, "Principles of Semiconductor Devices": [link]